

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 32

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHI-HWEY CHANG, YOSHITAKA UTSUMI,
GIOVANNI VANNUCCI, STEPHEN A. WILKUS
and GREGORY A. WRIGHT

Appeal No. 2002-1194
Application No. 08/534,808

ON BRIEF

Before THOMAS, BARRETT and SAADAT, Administrative Patent Judges.
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1, 2, 4-14, 16, 17 and 25-32. Claims 3, 15, 18-24 and 33 have been cancelled.

We reverse.

BACKGROUND

Appellants' invention is directed to a method for providing wireless transmission of information in electronic display systems and achieving synchronization in such systems. According to Appellants, values for bit and frame duration during a down-

link burst and up-link communication are chosen such that the display system has an opportunity to "sleep" for most of the duration of a frame and "wakes up" in time to receive the next frame with its local clock still synchronized (specification pages 16 and 17).

Representative independent claim 1 is reproduced below:

1. A method of achieving synchronization in an electronic display system having a communication base station and at least one electronic display module for displaying price or other product information, said method comprising the steps of:

(a) designating one preselected bit position in multiple bit messages to be transmitted from said communication base station to said at least one electronic display module with a value of zero;

(b) transmitting a plurality of said multiple bit messages in successive frames to said at least one electronic display module, said plurality of messages including guard band partition, address partition, command partition, synchronization partition, message information partition and parity check partition;

(c) said at least one electronic display module receiving said multiple bit messages from said communication base station;

(d) comparing each bit position in said multiple bit messages received;

(e) assigning a value of one if any one of said multiple bit messages has a one in a particular bit position;

(f) assigning a value of zero if all of said multiple bit messages has a zero in a particular bit position;

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(g) adjusting synchronization to position said value of zero in its proper orientation within said multiple bit messages based on the first remaining value of zero; and

(h) receiving an up-link message indicating synchronization has been achieved using a continuous wave tone.

The Examiner relies on the following reference in rejecting the claims:

"British Post Office standard" document (POCSAG), 1979.

Claims 1, 2, 4-14, 16, 17 and 25-32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over POCSAG.

We make reference to the answer (Paper No. 24, mailed October 20, 2000) for the Examiner's reasoning, and to the appeal brief (Paper No. 23, filed August 18, 2000) for Appellants' arguments thereagainst.

OPINION

The Examiner relies on section 3.3.1 of POCSAG for showing a "zero" in the bit position 32 of the synch codeword and asserts that "the signal needs to be resynched if the synch codeword does not match what is expected" or a "zero" is not in position 32 (answer, page 4). The Examiner further argues that shifting "the location of the zero bits in the synch bit to fit the claimed positions" is well known and its implementation would have been

obvious since the operation of the system would not have changed (id.).

Appellants argue that POCSAG discloses a recommended standard for radiopaging systems wherein each transmission starts with a preamble for attaining bit synchronization and preparing for acquiring word synchronization (brief, page 8). While acknowledging that the table in section 3.3.1 of POCSAG shows synchronization codewords having 32 bits and the value of the bit in position 32 to be "zero" (id.), Appellants argue that this limited evidence does not teach all of the claimed limitations (brief, page 9). Additionally, Appellants assert that the portion of the specification at page 28 is discussed in order to describe the claimed limitations that were not considered by the Examiner (brief, page 10).

In response to Appellants' arguments, the Examiner asserts that Appellants' arguments are merely general allegations "without specifically pointing out how the language of the claims patentably distinguishes them from the references [sic]" (answer, page 4). Additionally, for the first time in the prosecution, the Examiner outlines a more detailed rejection of claim 1 in the answer and explains how the alleged teachings in POCSAG would have suggested the claimed limitations (answer, pages 5-8).

Initially, we note that in rejecting claims under 35 U.S.C. § 103, it is the Examiner who bears the initial burden of presenting a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). Furthermore, in considering the question of the obviousness of the claimed invention in view of the prior art relied upon, the Examiner is expected to make the factual determination set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. See also In re Rouffet, 149 F.3d 1350, 1355, 47 USPQ2d 1453, 1456 (Fed. Cir. 1998). Here, this burden was not satisfied until the Examiner's Answer pointed to the teachings in POCSAG that allegedly read on each claimed limitation. Appellants are not required to provide evidence of patentability until this burden is shifted and therefore, prior to this point, could not reasonably be expected to speculate the Examiner's position and provide a convincing rebuttal.

Nevertheless, our review of POCSAG reveals that, as recognized by Appellants (brief, page 8), the reference relates to standardized code format for large capacity wide-area

radiopaging systems. Each transaction starts with a preamble to permit bit synchronization and prepare the pagers for word synchronization (section 3.1 Preamble). Codewords are transmitted in batches each of which includes a synchronization codeword, address codewords to identify each pager and message codeword directly following the related address codeword (section 3.2 Batch Structure). POCSAG further discloses that the first bit of the address codeword is always zero for distinguishing it from a message codeword (section 3.3.2 Address Codewords) which reads on the claimed value of zero for a preselected bit position.

Additionally, as depicted in Fig. 2 of POCSAG, a plurality of multiple bit messages in the form of a codeword format includes different sections or partitions labeled address bits, message bits, and parity check bits. However, contrary to the Examiner's position that guard band and command partitions are also included in the codeword format of Fig. 2 (answer, page 6), there is no teaching or suggestion in POCSAG that the codeword format includes all the listed elements, in particular, the claimed guard band and command partitions.

Furthermore, with regard to the last two steps in claim 1, the examiner neither points to, nor do we find any, specific

teachings in POCSAG that would have taught or suggested adjusting synchronization to position the value of zero in its proper orientation based on the first remaining value of zero. The Examiner merely concludes that shifting and comparing must be necessarily performed in order to recognize a synchronization codeword (answer, page 8) without providing factual evidence in support of such statement. In fact, POCSAG does not recognize the importance of positioning the value of zero in its proper orientation wherein the value of zero is assigned if all of the multiple bit messages have a zero in a particular bit position, as recited in steps (f) and (g) of claim 1.

In view of our analysis above, we find that the Examiner has failed to set forth a prima facie case of obviousness with respect to claim 1 and the other independent claims 9 and 25 as the necessary teachings and suggestions related to the claimed guardband and command partitions and adjusting the synchronization are not shown. Accordingly, we do not sustain the 35 U.S.C. § 103 rejection of independent claims 1, 9 and 25, nor of claims 2, 4-8, 10-14, 16, 17 and 26-32 dependent thereon.

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CONCLUSION

In view of the foregoing, the decision of the Examiner
rejecting claims 1, 2, 4-14, 16, 17 and 25-32 under 35 U.S.C.
§ 103 is reversed.

REVERSED

JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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MAHSHID D. SAADAT)	
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